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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,523	05/22/2001	Steven Derrick Clynes	TI-32423	1218

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EXAMINER	
MOE, AUNG SOE	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,523	CLYNES ET AL.	
	Examiner	Art Unit	
	Aung S. Moe	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 8 and 9 are objected to because of the following informalities:

In claim 8, line 3, the phrase "**the** lowest pixel value" should be changed to - - **a** lowest pixel value - -, because the phrase "lowest pixel value" was not presented in either claims 1, 6 or 7.

In claim 9, line 3, the phrase "**the** highest pixel value" should be changed to - - **a** highest pixel value - -, because the phrase "highest pixel value" was not presented in either claims 1, 2, or 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-11 and 14-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Chen et al. (EP 1,045,578 A2).

Regarding claim 1, Chen '578 discloses a method of pixel filtering for CMOS imagers (Figs. 1 & 2; col. 4, lines 35+), comprising: scanning each of a plurality of pixels within a block (i.e., noted the pixel block as shown in Fig. 4a-4c; col. 7, lines 10+); designating a pixel as a process pixel (i.e., noted the B pixels as shown in Figs. 3a-4c; see col. 7, lines 10+), the process pixel having adjacent pixels (i.e., noted the A and C pixels as shown in Figs. 3a-4c; see col. 7, lines 10), the process pixel having a process pixel value (i.e., noted the pixel value of the middle pixel B as shown in Figs. 3a-4c; see col. 7, lines 10+), each of the adjacent pixels having an adjacent pixel value (i.e., noted the pixel values of the adjacent pixels A and B as shown in Figs. 3a-4c; see col. 7, lines 1+); and comparing the process pixel value to at least one adjacent pixel value (i.e., col. 6, lines 30+, col. 7, lines 1+, col. 8, lines 5+).

Regarding claim 2, Chen '578 discloses further comprising detecting a lowest pixel value among the adjacent pixels (i.e., as shown in Figs. 3a-3j, the lowest pixel values of the adjacent pixels A and C are respectively determined by the imaging logic 8; see col. 6, lines 30+, col. 7, lines 10+ and col. 8, lines 5+ and col. 9, lines 45+).

Regarding claim 3, Chen '578 discloses wherein comparing compares the process pixel value to a lowest pixel value (as shown in Figs. 3a-3j, the defective-pixel filter 34 of the imaging logic 8 compared the lowest pixel value of the adjacent pixels A/C with the middle pixels B; see col. 8, lines 1+ and col. 9, lines 15+).

Regarding claim 4, Chen '578 discloses further comprising resetting the process pixel to a new pixel value (i.e., as discussed in col. 9, lines 45+, that if the condition of the pixel values are determined to be as shown in Figs. 3g and 3j, then the process pixel B is reset, e.g., replaced, by a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 5, Chen '578 discloses wherein the new pixel value is the average pixel value of the adjacent pixel values (i.e., col. 9, lines 50+).

Regarding claim 6, Chen '578 discloses further comprising detecting a highest pixel value among the adjacent pixels (i.e., noted the pixel values of pixel 54 as shown in Figs. 3g and 3j).

Regarding claim 7, Chen '578 discloses wherein comparing compares the process pixel value to a highest pixel value (i.e., noted form Figs. 3a-3j and 5 that the defective-pixel filter 34 of the imaging logic 8 compared the highest pixel value of the adjacent pixels A/C with the middle pixels B; see col. 8, lines 1+ and col. 9, lines 15+).

Regarding claim 8, Chen '578 discloses further comprising resetting (i.e., Replacing the pixel value B with a new pixel value $B_{corrected}$; see col. 9, lines 45+) the process pixel value (i.e., the B pixel value as shown in Fig. 3j) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3j) lower than the lowest pixel value (noted form Fig. 3j, a predetermined value is lower than the lowest pixel value A, then the pixel value B is replaced with a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 9, Chen '578 discloses further comprising resetting the process pixel value (i.e., Replacing the pixel value B with a new pixel value $B_{corrected}$; see col. 9, lines 45+)

when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3g) greater than the highest pixel value (noted form Fig. 3g, a predetermined value is greater than the highest pixel value C, then the pixel value B is replaced with a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 10, Chen '578 discloses further comprising exposing an array to a light source so as to cast an image on the array (Fig. 1, the sensor array 6; col. 5, lines 20+), the array having at least one block (i.e., noted the block as shown in Fig. 4).

Regarding claim 11, Chen '578 discloses wherein the array is generally grid-shaped (i.e., noted that an array of CMOS sensor cells contain a matrix of pixel array generally formed as a grid-shape).

Regarding claim 14, Chen '578 discloses a chip that automatically filters defective pixels in a CMOS imager (i.e., Figs. 1-5; col. 6, lines 10+), comprising:

a plurality of registers (i.e., Fig. 2, the elements 22, 24, and 32); and filter logic (34) coupled to the registers (i.e., col. 5, lines 25+ and col. 6, lines 30+).

Regarding claim 15, Chen '578 discloses wherein the filter logic (34) is capable of: designating a pixel as a process pixel (i.e., noted that the pixel B is designated by the filter logic 34 as a process pixel; see col. 6, lines 30+ and col. 7, lines 1), the process pixel having adjacent pixels (i.e., noted the pixels A and C as shown in Figs. 3a-3j), the process pixel having a process pixel value (i.e., noted the pixel values of pixel B as shown in Figs. 3a-3j), each of the adjacent pixels having an adjacent pixel value (i.e., noted the pixel values of the adjacent pixels A and B

as shown in Figs. 3a-4c; see col. 7, lines 1+); and comparing the process pixel value to at least one adjacent pixel value (i.e., Fig. 5; col. 6, lines 30+, col. 7, lines 1+, col. 8, lines 5+).

Regarding claim 16, Chen '578 discloses further comprising an array (i.e., noted the sensor array 6) coupled to the registers (i.e., see Fig. 2).

Regarding claim 17, Chen '578 discloses a method of on-chip pixel filtering for CMOS imagers (Figs. 1 & 2; col. 4, lines 35+), comprising:

scanning each of a plurality of pixels within a block for a pixel value (i.e., see Figs. 3a-4c; col. 7, lines 5+); loading a pixel value into a register (Fig. 5; col. 7, lines 35+ and col. 8, lines 5+); using filter logic (34) to designate a pixel as a process pixel (i.e., noted that the pixel B is designated by the filter logic 34 as a process pixel; see col. 6, lines 30+), the process pixel having adjacent pixels (i.e., noted the pixels A and C as shown in Fig. 3a-4c), the process pixel having a process pixel value (i.e., noted the process pixel values of pixel B as shown in Figs. 3a-3j), each of the adjacent pixels having an adjacent pixel value (i.e., noted the pixel values of the adjacent pixels A and B as shown in Figs. 3a-4c; see col. 7, lines 1+); and using filter logic (34) to compare the process pixel value to at least one adjacent pixel value.

Regarding claim 18, Chen '578 discloses wherein the filter logic compares the process pixel value to a highest pixel value, further comprising: detecting the highest pixel value among the adjacent pixels; and resetting the process pixel value to a new process pixel value when the process pixel value is a predetermined value higher than the highest pixel value (i.e., Fig. 5; col. 6, lines 30+, col. 7, lines 1+, col. 8, lines 5+).

Regarding claim 19, Chen '578 discloses wherein the filter logic (34) compares the process pixel value (i.e., the middle pixel value B as shown in Figs. 3g and 3j) to a lowest pixel value (i.e., noted the lowest pixel value A as shown in Figs. 3g and 3j), further comprising: detecting the lowest pixel value among the adjacent pixels (i.e., noted from Figs. 3a-3j, the lowest pixel values are determined by the filter logic 34 and the system controller 28); and resetting the process pixel value to a new process pixel value (i.e., Replacing the pixel value B with a new pixel value $B_{corrected}$; see col. 9, lines 45+) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3j) lower than the lowest pixel value (noted form Fig. 3j, a predetermined value is lower than the lowest pixel value A, then the pixel value B is replaced with a new pixel value $B_{corrected}$; see col. 9, lines 45+).

Regarding claim 20, Chen '578 discloses wherein the new process pixel value is the average pixel value of the adjacent pixel values (i.e., see col. 9, lines 45+).

4. Claims 1, 6-7, 10-13 and 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Mahant-Shetti et al. (U.S. 6,529,238 B1).

Regarding claim 1, Mahant-Shetti '238 discloses a method of pixel filtering for CMOS imagers (Figs. 2 and 5; see col. 2, lines 30+; col. 4, lines 46+ and col. 5, lines 15+), comprising:

scanning each of a plurality of pixels within a block (i.e., see col. 5, lines 65+);

designating a pixel as a process pixel (i.e., noted the use of a current pixel; see col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+), the process pixel having adjacent pixels (i.e., noted the surrounding pixels as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines

45+), the process pixel (i.e., the current pixel) having a process pixel value (i.e., noted that the current pixel values as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+), each of the adjacent pixels having an adjacent pixel value (i.e., noted the surrounding pixels values as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+); and

comparing the process pixel value to at least one adjacent pixel value (i.e., col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+).

Regarding claim 6, Mahant-Shetti '238 discloses further comprising detecting a highest pixel value (i.e., noted the maximum pixel values of the 8 surrounding pixels) among the adjacent pixels (i.e., see col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+).

Regarding claim 7, Mahant-Shetti '238 discloses wherein comparing compares the process pixel value to a highest pixel value (i.e., see col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+).

Regarding claim 10, Mahant-Shetti '238 discloses further comprising exposing an array to a light source (i.e., noted the CMOS sensor array 201) so as to cast an image on the array (i.e., see col. 5, lines 24+), the array having at least one block (i.e., col. 5, lines 65-68).

Regarding claim 11, Mahant-Shetti '238 discloses wherein the array is generally grid-shaped (i.e., see col. 5, lines 24-30).

Regarding claim 12, Mahant-Shetti '238 discloses wherein the block is generally grid-shaped (i.e., noted the use of 3 x 3 pixels grid as discussed in col. 5, lines 65+).

Regarding claim 13, Mahant-Shetti '238 discloses wherein the block has nine pixels (i.e., noted the use of 3 x 3 pixels grid as discussed in col. 5, lines 65+).

Regarding claim 14, Mahant-Shetti '238 discloses a chip that automatically filters defective pixels in a CMOS imager (Figs. 2 and 5; col. 6, lines 1-55), comprising:

a plurality of registers (i.e., noted the registers 203; see col. 5, lines 45+); and filter logic (i.e., as shown in Figs. 2 and 5, the defect pixel is filtered by the logic circuits 204-206 and 501) coupled to the registers (i.e., the element 203 having 3 x N registers).

Regarding claim 15, Mahant-Shetti '238 discloses wherein the filter logic is capable of: designating a pixel as a process pixel (i.e., noted the use of a current pixel; see col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+), the process pixel having adjacent pixels (i.e., noted the surrounding pixels as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+), the process pixel having a process pixel value (i.e., noted that the current pixel values as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+), each of the adjacent pixels having an adjacent pixel value (i.e., noted the surrounding pixels values as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+); and comparing the process pixel value to at least one adjacent pixel value (i.e., col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+).

Regarding claim 16, Mahant-Shetti '238 discloses further comprising an array (i.e., noted the sensor array 201) coupled to the registers (203).

Regarding claim 17, Mahant-Shetti '238 discloses a method of on-chip pixel filtering for CMOS imagers (Fig. 2 and 5), comprising:

scanning each of a plurality of pixels within a block for a pixel value (i.e., col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+);

loading a pixel value into a register (203); using filter logic (i.e., the elements 204-206 and 501) to designate a pixel as a process pixel (i.e., noted the use of a current pixel), the process pixel having adjacent pixels (i.e., noted the 8 surrounding pixels; see col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+), the process pixel having a process pixel value, each of the adjacent pixels having an adjacent pixel value (i.e., noted the value of the current pixel and the 8 surrounding pixels as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+); and

using filter logic (i.e., the elements 204-206 and 501) to compare the process pixel value to at least one adjacent pixel value (i.e., col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+).

Regarding claim 18, Mahant-Shetti '238 discloses wherein the filter logic compares the process pixel value to a highest pixel value (i.e., the maximum pixel values as discussed in col. 4, lines 50+, col. 6, lines 60+ and col. 7, lines 45+), further comprising: detecting the highest pixel value among the adjacent pixels (i.e., noted that the maximum signals of the surrounding pixels are determined by the logic circuits 204-206 and 501; col. 4, lines 50+, col. 6, lines 30+ and col. 7, lines 45+); and resetting the process pixel value to a new process pixel value when the process pixel value is a predetermined value higher than the highest pixel value (i.e., replacing the current pixel value with the new pixel value; col. 4, lines 45+, col. 6, lines 60+ and col. 7, lines 45+).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Matsukawa '614, Levine '579, Hsu '139 and Rambaldi '488 shown the system and method for correcting a defective pixel in the imaging device.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 703-306-3021. The examiner can normally be reached on Mon-Fri (9-5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aung S. Moe
Primary Examiner
Art Unit 2612

A. Moe
August 6, 2004